

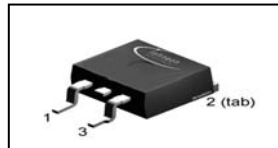
OptiMOS[®] -T Power-Transistor
Features

- N-channel - Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

Product Summary

| | | |
|--------------------------------|-----|------------|
| V_{DS} | 55 | V |
| $R_{DS(on),max}$ (SMD version) | 3.5 | m Ω |
| I_D | 100 | A |

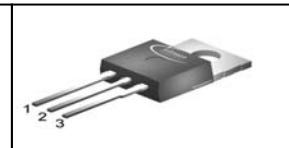
PG-TO263-3-2



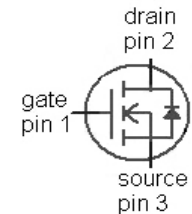
PG-TO262-3-1



PG-TO220-3-1



| Type | Package | Ordering Code | Marking |
|-----------------|--------------|---------------|----------|
| IPB100N06S3L-04 | PG-TO263-3-2 | SP0001-02219 | 3PN06L04 |
| IPI100N06S3L-04 | PG-TO262-3-1 | SP0001-02211 | 3PN06L04 |
| IPP100N06S3L-04 | PG-TO220-3-1 | SP0001-02209 | 3PN06L04 |


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|-------------------|--|--------------|------|
| Continuous drain current ¹⁾ | I_D | $T_C=25\text{ °C}$, $V_{GS}=10\text{ V}$ | 100 | A |
| | | $T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^2)$ | 100 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | 400 | |
| Avalanche energy, single pulse ³⁾ | E_{AS} | $I_D=50\text{ A}$ | 450 | mJ |
| Drain gate voltage ²⁾ | V_{DG} | | 55 | V |
| Gate source voltage ⁴⁾ | V_{GS} | | ± 16 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 214 | W |
| Operating and storage temperature | T_j , T_{stg} | | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | | | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|--|------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics²⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | | - | - | 0.7 | K/W |
| Thermal resistance, junction - ambient, leaded | R_{thJA} | | - | - | 62 | |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ⁵⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|---|-----|------|-----|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=1\text{ mA}$ | 55 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=150\text{ }\mu\text{A}$ | 1.2 | 1.6 | 2.2 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$ | - | 0.01 | 1 | μA |
| | | $V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}^{2)}$ | - | 1 | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=16\text{ V}, V_{DS}=0\text{ V}$ | - | 1 | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=5\text{ V}, I_D=59\text{ A}$ | - | 4.9 | 6.2 | m Ω |
| | | $V_{GS}=5\text{ V}, I_D=59\text{ A},$ SMD version | - | 4.6 | 5.9 | |
| | | $V_{GS}=10\text{ V}, I_D=80\text{ A}$ | - | 3.1 | 3.8 | |
| | | $V_{GS}=10\text{ V}, I_D=80\text{ A},$ SMD version | - | 2.8 | 3.5 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|--|---|-------|---|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$ | - | 17270 | - | pF |
| Output capacitance | C_{oss} | | - | 2165 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 2070 | - | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=80\text{ A},$ $R_G=2\ \Omega$ | - | 30 | - | ns |
| Rise time | t_r | | - | 58 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 82 | - | |
| Fall time | t_f | | - | 55 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|--|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=11\text{ V}, I_D=80\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$ | - | 71 | - | nC |
| Gate to drain charge | Q_{gd} | | - | 45 | - | |
| Gate charge total | Q_g | | - | 241 | 362 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.8 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|-----|-----|-----|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 100 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | | - | - | 400 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_J=25\text{ }^\circ\text{C}$ | 0.6 | 0.9 | 1.3 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$ | - | - | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | - | - | |

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.7\text{ K/W}$ the chip is able to carry 176 A at 25°C. For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design. Not subject to production test.

³⁾ See diagrams 12 and 13.

⁴⁾ Qualified at -5V and +16V.

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

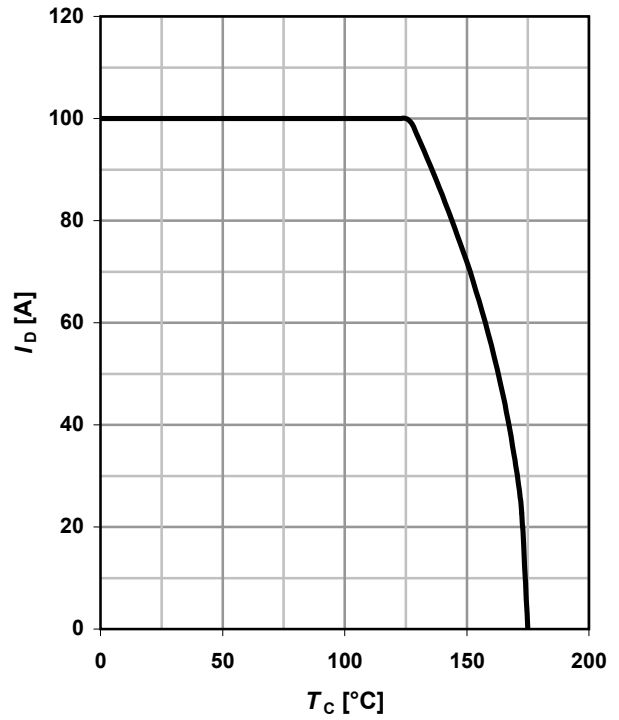
1 Power dissipation

$P_{tot}=f(T_C); V_{GS} \geq 4\text{ V}$



2 Drain current

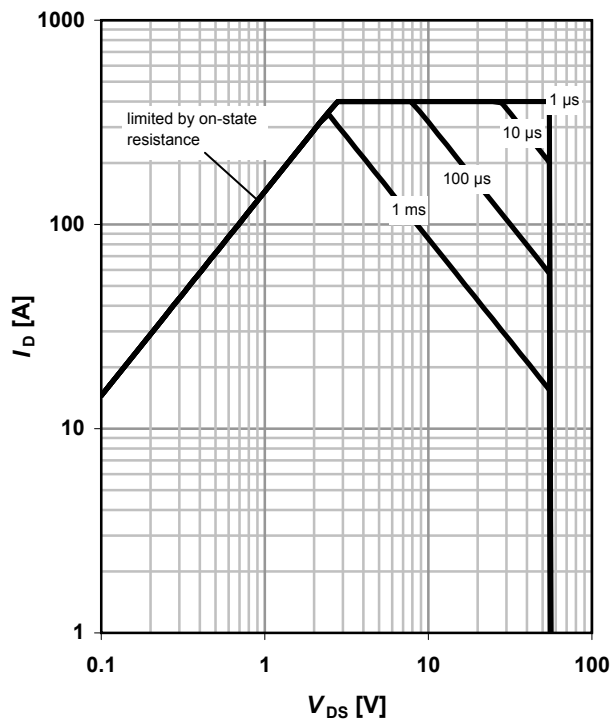
$I_D=f(T_C); V_{GS} \geq 4\text{ V}$



3 Safe operating area

$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$

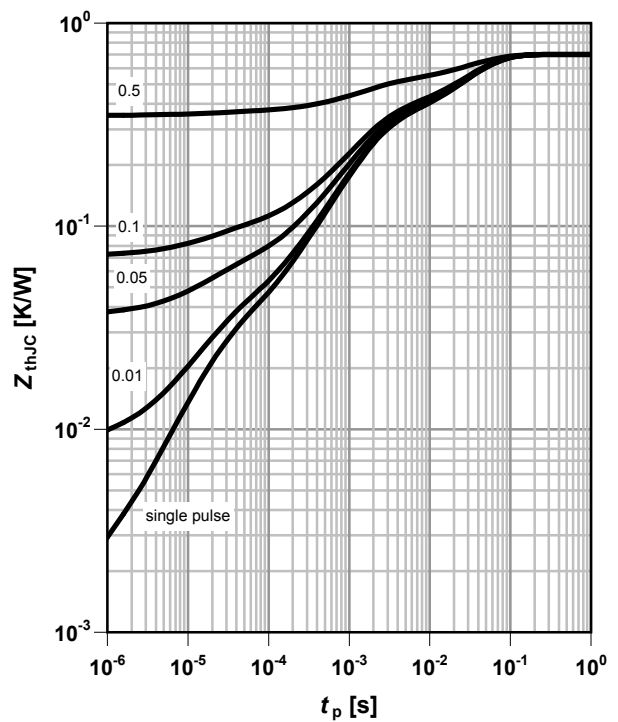
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$

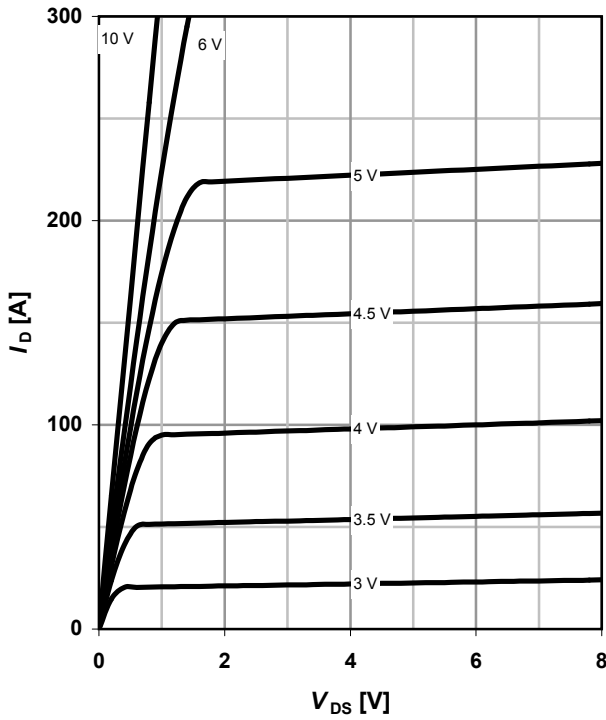
parameter: $D=t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

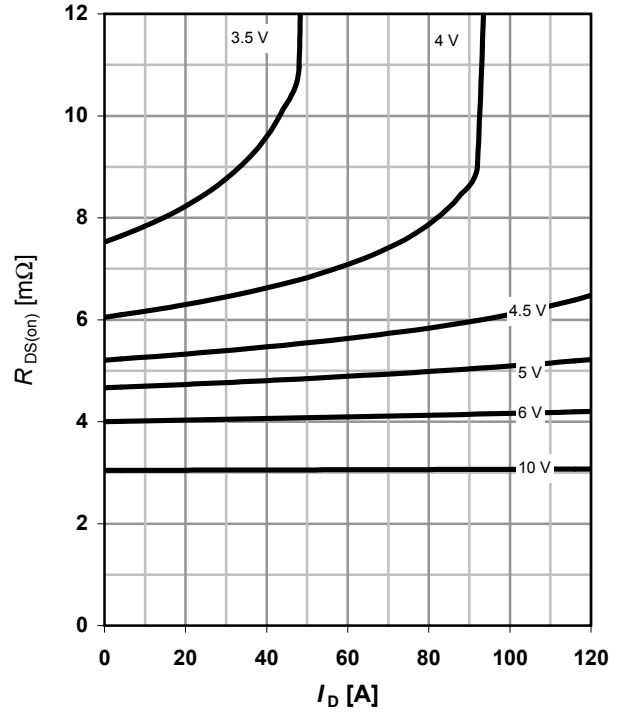
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

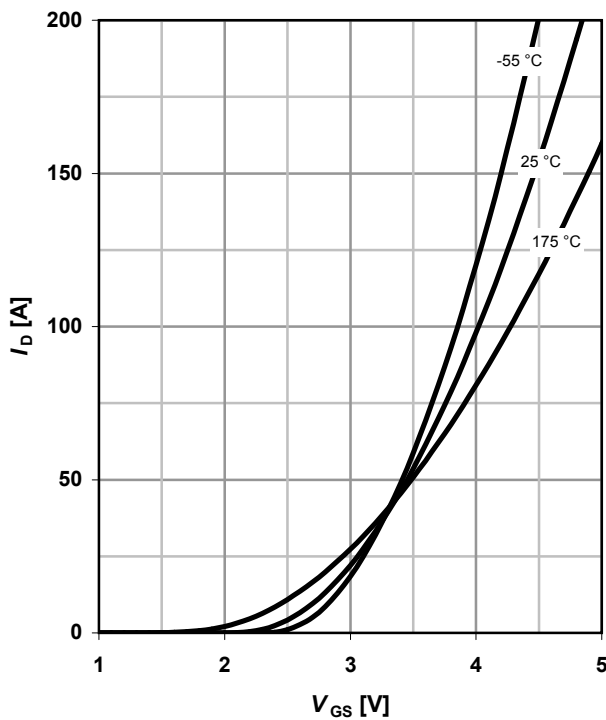
parameter: V_{GS}



7 Typ. transfer characteristics

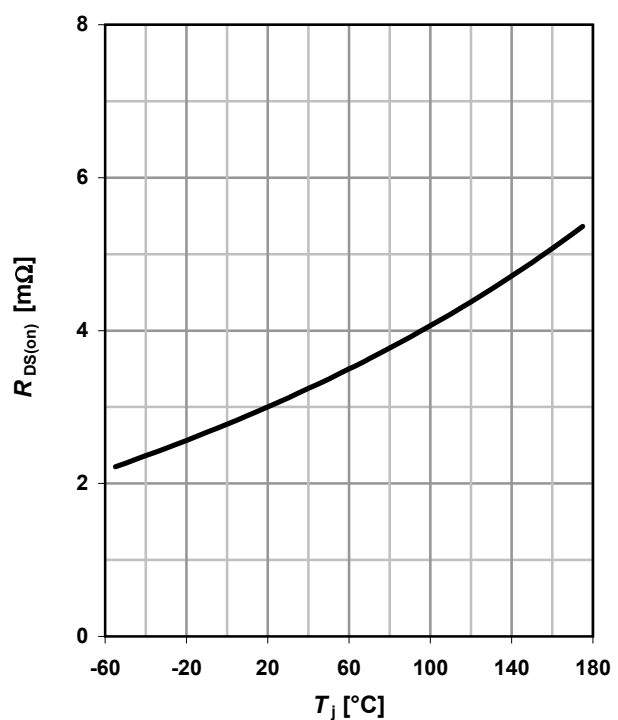
$I_D = f(V_{GS}); V_{DS} = 4\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

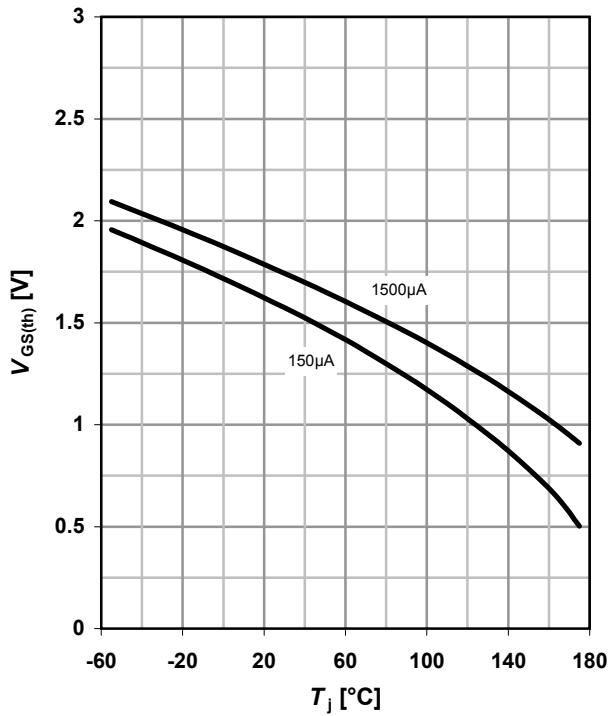
$R_{DS(on)} = f(T_j); I_D = 80\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

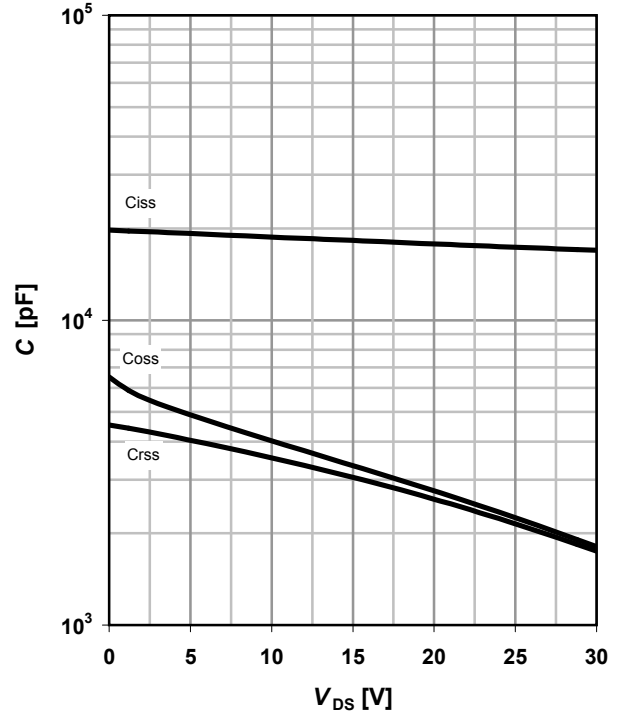
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

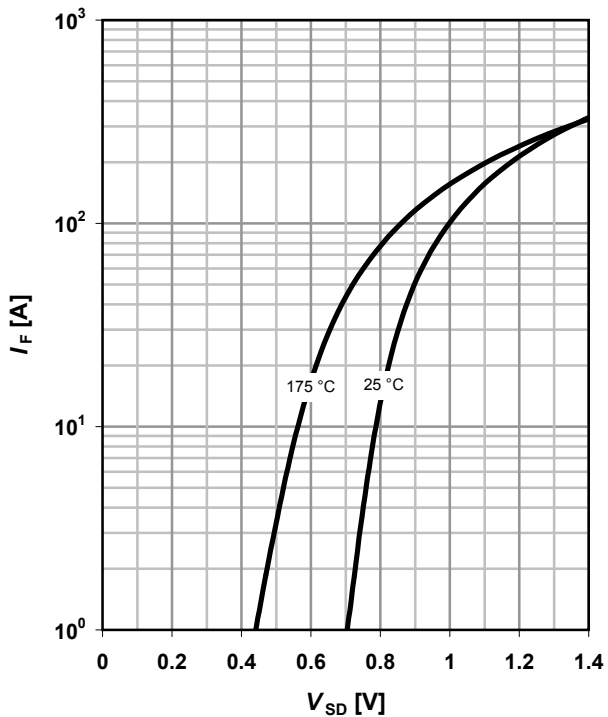
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

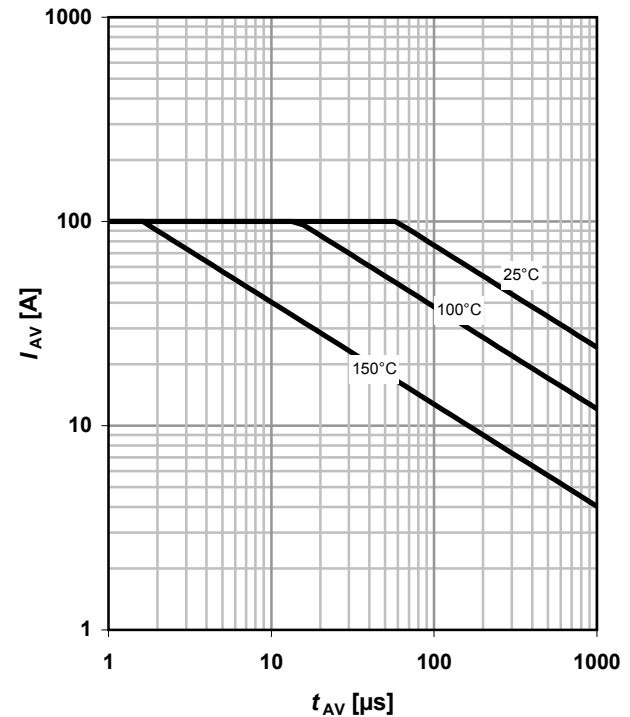
parameter: T_j



12 Typ. avalanche characteristics

$I_{AV} = f(t_{AV})$

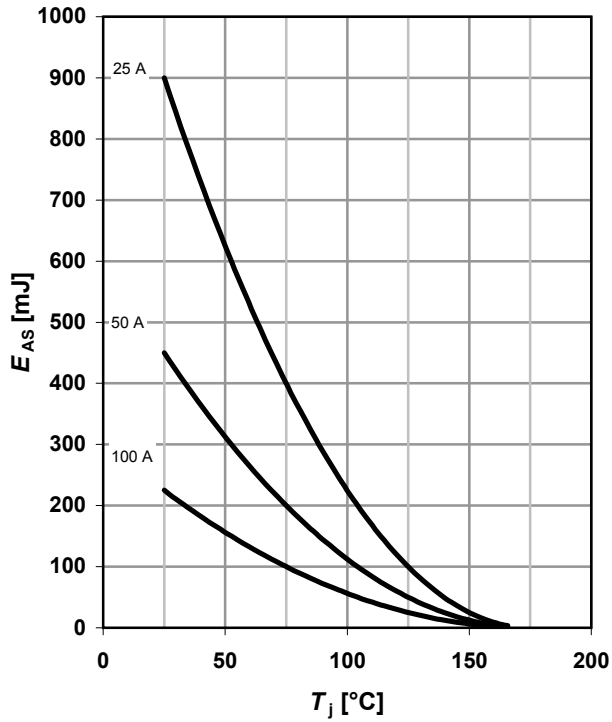
parameter: $T_{j(start)}$



13 Typical avalanche energy

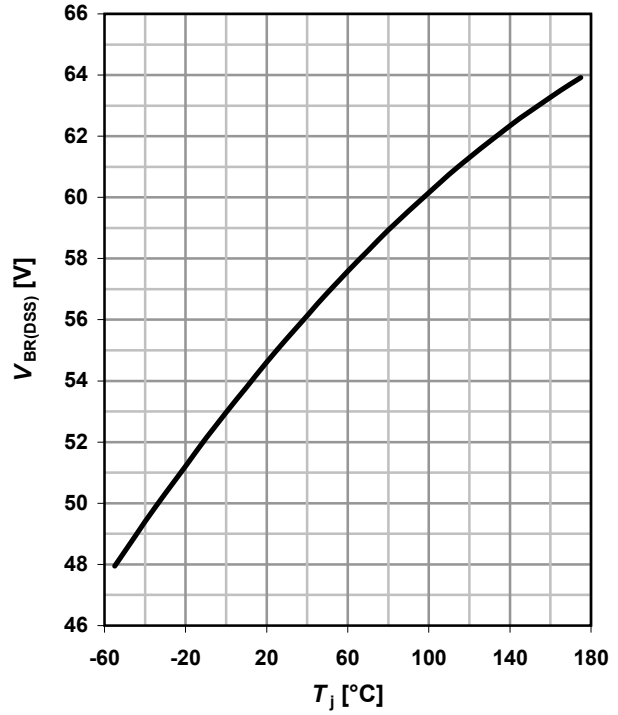
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

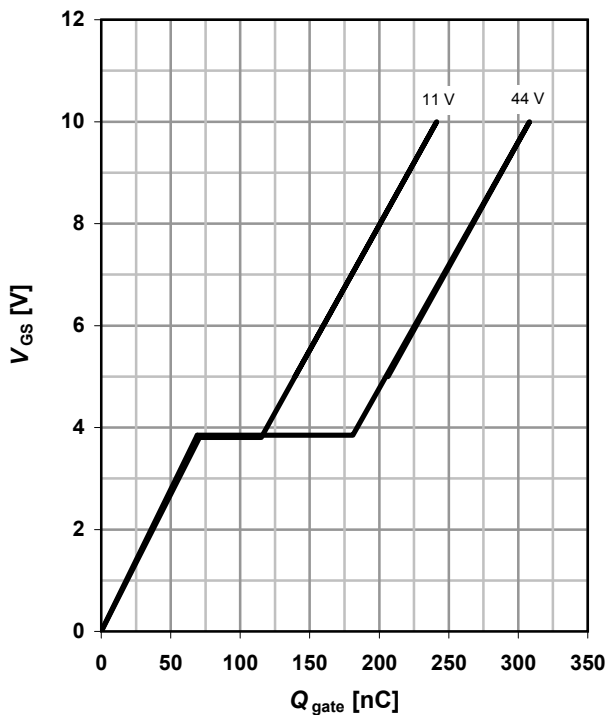
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



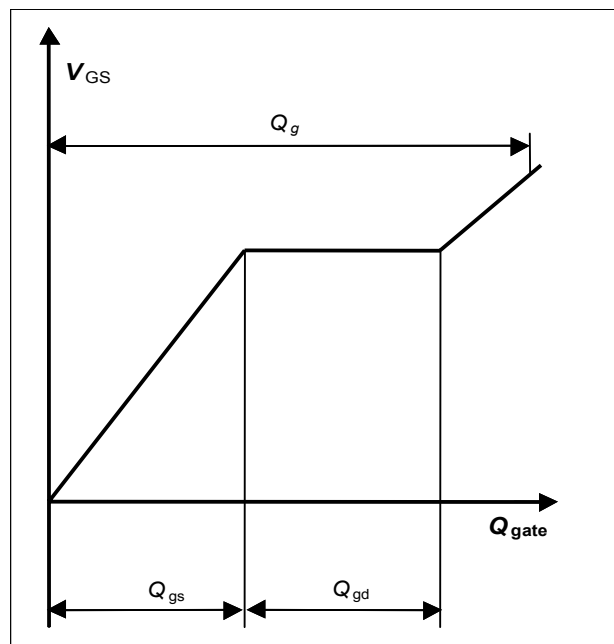
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 80 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Published by
Infineon Technologies AG
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D-81541 München
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